RS1G74-Q1 Single Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset

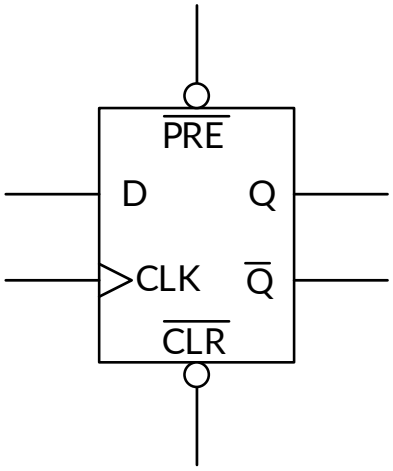
1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **Operating Voltage Range:1.65V to 5.5V**
- **Low Power Consumption:10μA (Max)**
- **Operating Temperature Range: -40°C to +125°C**
- **Inputs Accept Voltage to 5.5V**
- **High Output Drive: ±24mA at V_{CC}=3.0V**
- **I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection**
- **Micro SIZE PACKAGES: VSSOP8**

2 APPLICATIONS

- **Automotive Infotainment**
- **Automotive Cluster**
- **Automotive ADAS**
- **Automotive Body Electronics**
- **Automotive HEV/EV Powertrain**

Simplified Schematic



3 DESCRIPTIONS

The RS1G74-Q1 single positive-edge-triggered D-type flip-flop is designed for 1.65V to 5.5V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The RS1G74-Q1 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

This device available in Green VSSOP8 packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1G74-Q1	VSSOP8	2.00mm×2.30mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2024/04/15	Preliminary version completed
A.1	2024/05/20	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS1G74 -Q1	RS1G74XVS8 -Q1	-40°C ~+125°C	VSSOP8	NIPDAUAG	MSL1-260°-Unlimited	1G74	Tape and Reel,3000

NOTE:

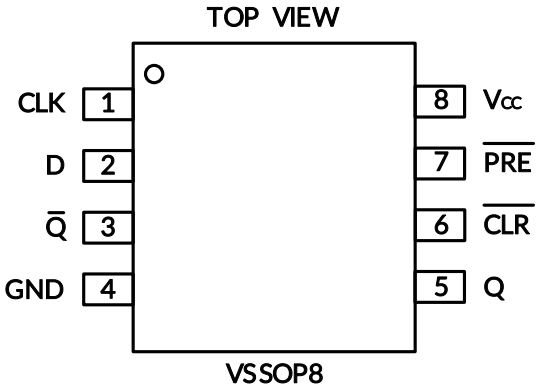
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) MSL Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

6 PIN CONFIGURATIONS



6.1 PIN DESCRIPTION

PIN	NAME	I/O TYPE (1)	FUNCTION
VSSOP8			
1	CLK	I	Clock Input
2	D	I	Input
3	$\overline{Q}$	O	Inverted output
4	GND	-	Ground
5	Q	O	Output
6	$\overline{CLR}$	I	Clear input-Pull low to set Q output low
7	$\overline{PRE}$	I	Preset input-pull low to set Q output high
8	V_{CC}	P	Supply

(1) I=input, O=output, P=power.

6.2 FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is non-stable, that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.
(2) H=High Voltage Level
L=Low Voltage Level
X=Don't Care

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2) (3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance (4)	VSSOP8		227	°C/W
T_J	Junction temperature (5)		-65	150	°C
Tstg	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-Device Model (CDM), per AEC Q100-011	±1000	V
		Latch-Up (LU), per AEC Q100-004	±150	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

8.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
High-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V	0.75 x V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2.3		
		V_{CC}=4.5V to 5.5V	0.7 x V_{CC}		
Low-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		0.25 x V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3 x V_{CC}	
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
High-level output current	I_{OH}	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
Low-level output current	I_{OL}	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Input transition rise or fall	Δt / Δv	V_{CC}=1.8V± 0.15V,2.5V ± 0.2V		20	ns/V
		V_{CC}=3.3V± 0.3V		10	
		V_{CC}=5V± 0.5V		10	
Operating temperature	T_A		-40	+125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

8.2 DC Characteristics

PARAMETER		TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}		I_{OH} = -100μA	1.65V to 5.5V	Full	V_{CC}-0.1			V
		I_{OH} = -4mA	1.65V		1.2			
		I_{OH} = -8mA	2.3V		1.9			
		I_{OH} = -16mA	3V		2.4			
		I_{OH} = -24mA			2.3			
		I_{OH} = -32mA	4.5V		3.8			
V_{OL}		I_{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I_{OL} = 4mA	1.65V				0.45	
		I_{OL} = 8mA	2.3V				0.3	
		I_{OL} = 16mA	3V				0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA	4.5V				0.55	
I_I	Data or control inputs	V_I=5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I_{off}		V_I or V_O=5.5V	0	+25°C		±0.1	±1	μA
				Full			±10	
I_{CC}		V_I=5.5V or GND, I_O=0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI_{CC}		One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	Full			500	μA
C_i (Input Capacitance)		V_I = V_{CC} or GND	3.3V	+25°C		5.5		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

8.3 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO(OUTPUT)	TEMP	V_{CC}=1.8V		V_{CC}=2.5V		V_{CC}=3.3V		V_{CC}=5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}			-40°C to 85°C		30		65		100		155	MHz
			-40°C to 125°C						100		155	
t_w	CLK		-40°C to 85°C	8		4		3		2		ns
			-40°C to 125°C					3		2		
	$\overline{PRE}$ or $\overline{CLR}$ low		-40°C to 85°C	12		5		3.4		2		
			-40°C to 125°C					3.4		2		
t_{su}	Data		-40°C to 85°C	10.4		4.6		3.2		2		
			-40°C to 125°C					3.2		2		
	$\overline{PRE}$ or $\overline{CLR}$ inactive		-40°C to 85°C	8.4		3.8		2.6		1.8		
			-40°C to 125°C					2.6		1.8		
t_h			-40°C to 85°C	0.5		0.5		0.5		0.5		
			-40°C to 125°C					0.5		0.5		

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.4 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO(OUTPUT)	TEMP	V_{CC}=1.8V		V_{CC}=2.5V		V_{CC}=3.3V		V_{CC}=5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			-40°C to 85°C	30		65		100		155		MHz
			-40°C to 125°C					100		155		
t_{pd}	CLK	Q	-40°C to 85°C	4.8	23.5	2.2	15.5	2.2	11.5	1.4	9.2	ns
			-40°C to 125°C					2.2	12.5	1.4	9.5	
		$\overline{Q}$	-40°C to 85°C	6	25.5	3	17	2.6	12.5	1.6	9.6	
			-40°C to 125°C					2.6	13.5	1.6	10	
	$\overline{PRE}$ or $\overline{CLR}$ low	Q or $\overline{Q}$	-40°C to 85°C	4.4	27	2.3	16	1.7	12	1.6	9.4	
			-40°C to 125°C					1.7	13	1.6	9.8	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.5 Operating Characteristics

T_A = +25°C

PARAMETER	TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	f = 10 MHz	22	25	32	40	pF

8.6 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, V_{CC}=3.3V, unless otherwise noted.

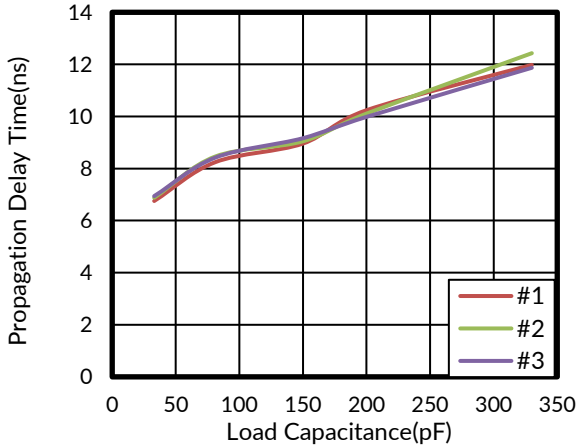


Figure 1. Propagation Delay (Low to High Transition) vs Load Capacitance

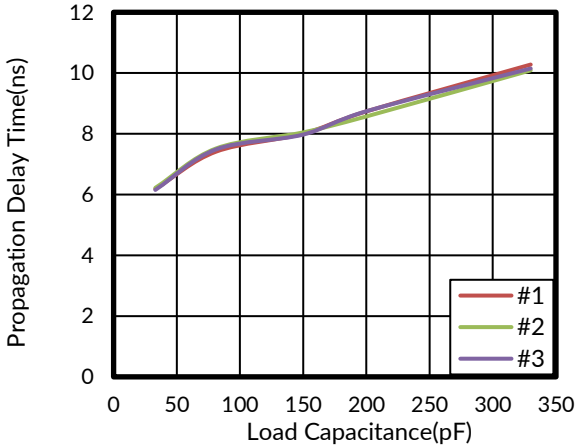
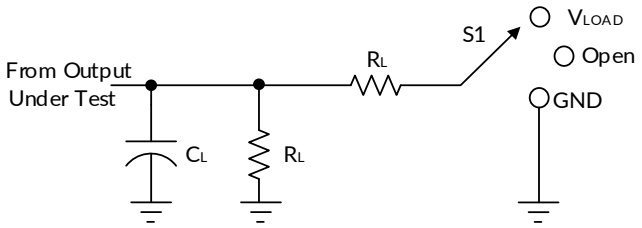


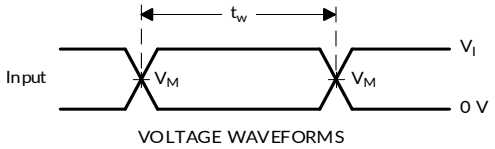
Figure 2. Propagation Delay (High to Low Transition) vs Load Capacitance

9 PARAMETER MEASUREMENT INFORMATION

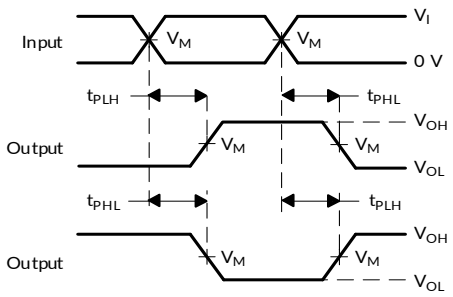


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

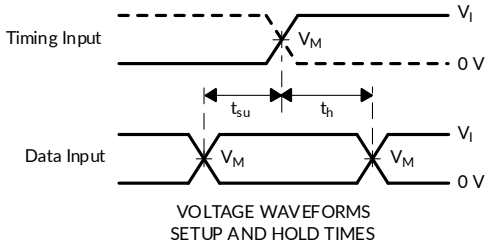
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	1kΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	50pF	500Ω	0.3V



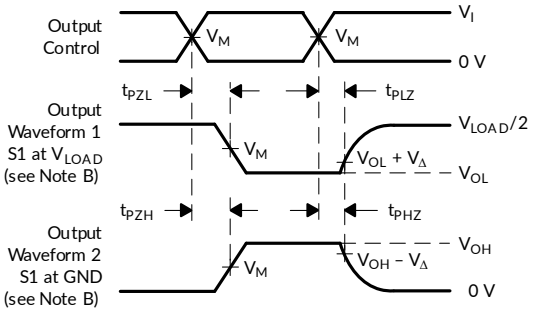
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY
TIMES INVERTION AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES
LOW-AND HIGH-LEVEL ENABLING

NOTES: A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

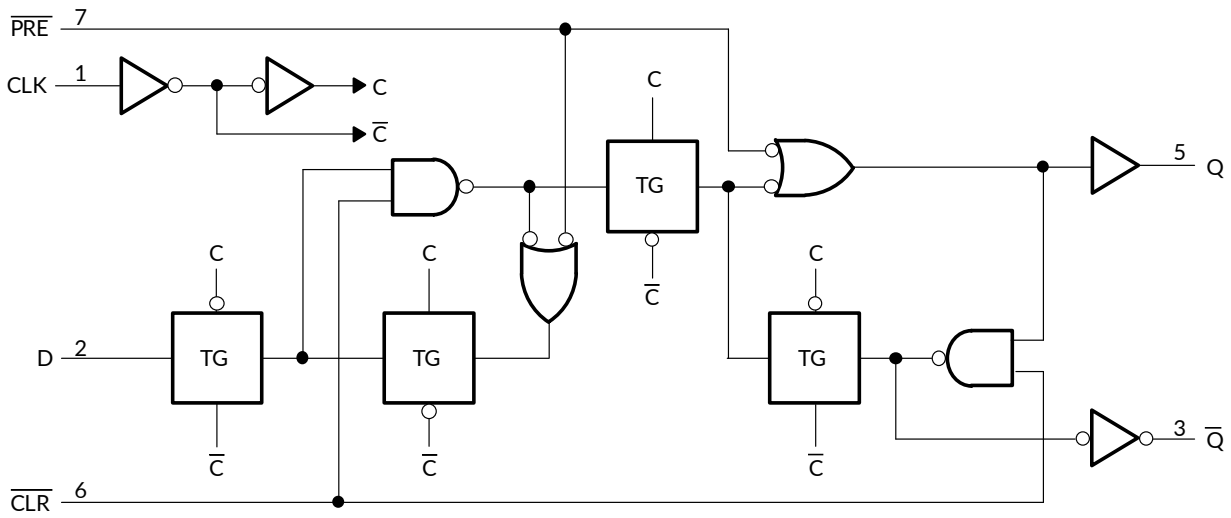
Figure 3. Load Circuit and Voltage Waveforms

10 DETAILED DESCRIPTION

10.1 Overview

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

10.2 Functional Block Diagram



11 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive(high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The resistor and capacitor at the $\overline{CLR}$ pin are optional. If they are not used, the $\overline{CLR}$ pin should be connected directly to V_{CC} to be inactive.

11.2 Typical Application (Power Button Circuit)

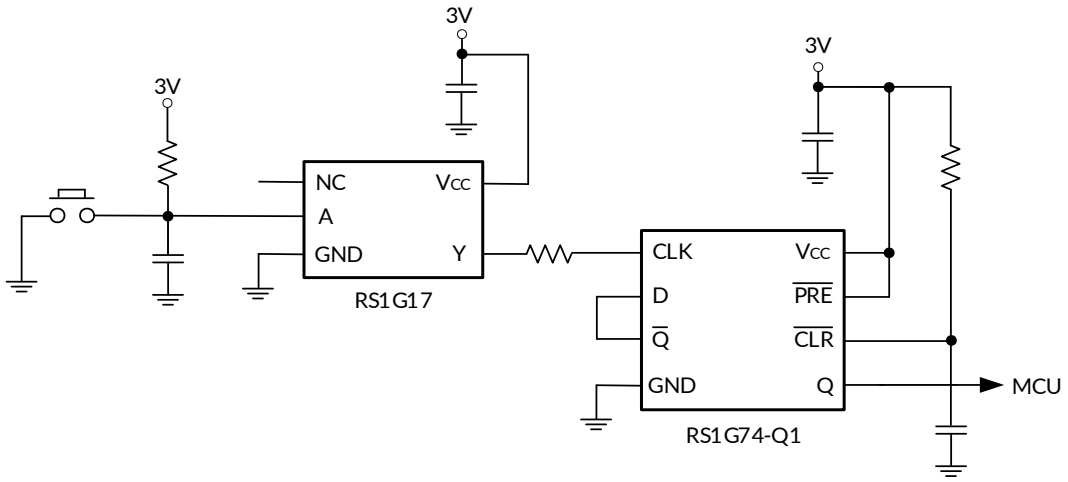


Figure 4. Device Power Button Circuit

11.3 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

12 POWER SUPPLY RECOMMENDATIONS

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1uF capacitor is recommended and if there are multiple V_{CC} terminals then 0.01uF or 0.022uF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

13 LAYOUT

13.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 5 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/O_S so they also cannot float when disabled.

13.2 Layout Example

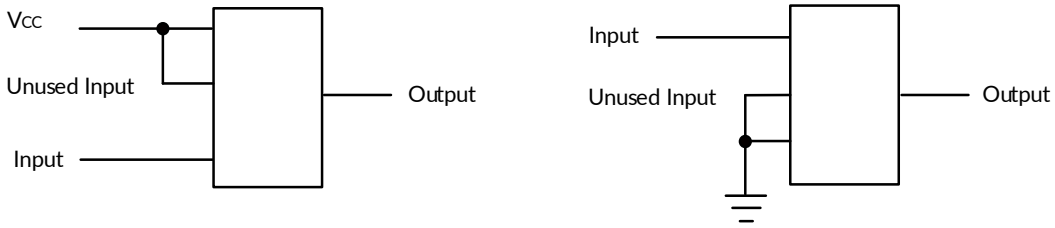
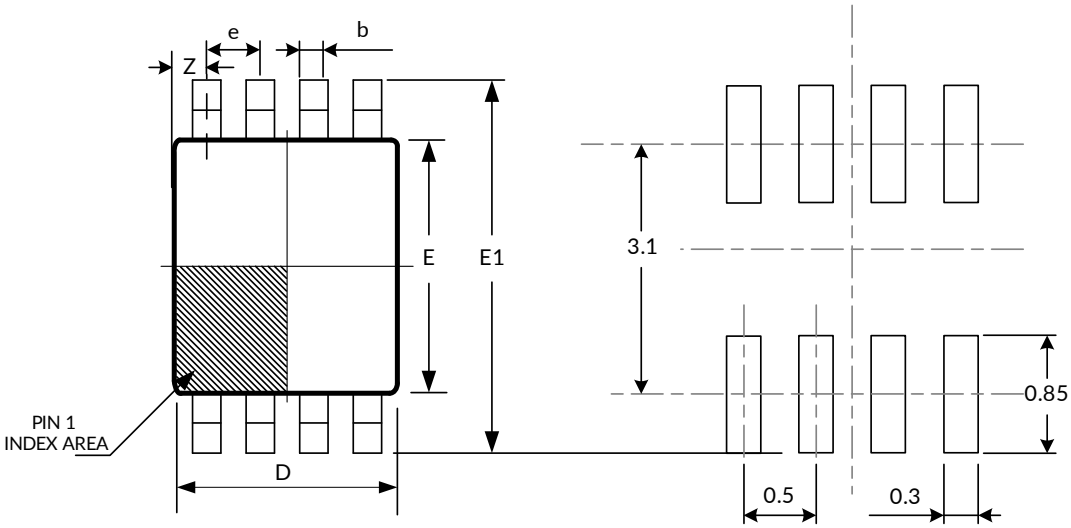


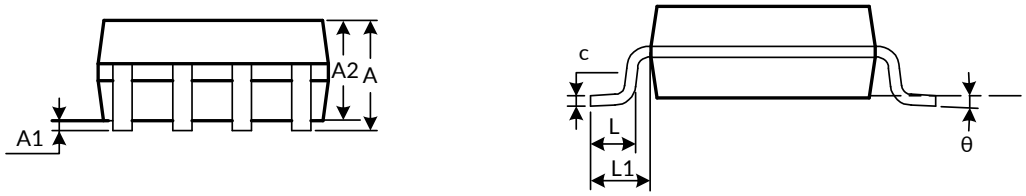
Figure 5. Layout Diagram

14 PACKAGE OUTLINE DIMENSIONS

VSSOP8 (3)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.000		0.039
A1	0.000	0.150	0.000	0.006
A2	0.600	0.850	0.023	0.034
b	0.170	0.270	0.007	0.010
c	0.080	0.230	0.003	0.009
D (1)	1.900	2.100	0.075	0.083
e	0.500 (BSC) (2)		0.020 (BSC) (2)	
E (1)	2.200	2.400	0.087	0.095
E1	3.000	3.200	0.118	0.126
L	0.150	0.400	0.006	0.016
L1	0.400 (BSC) (2)		0.016 (BSC) (2)	
Z	0.100	0.400	0.004	0.016
θ	0°	8°	0°	8°

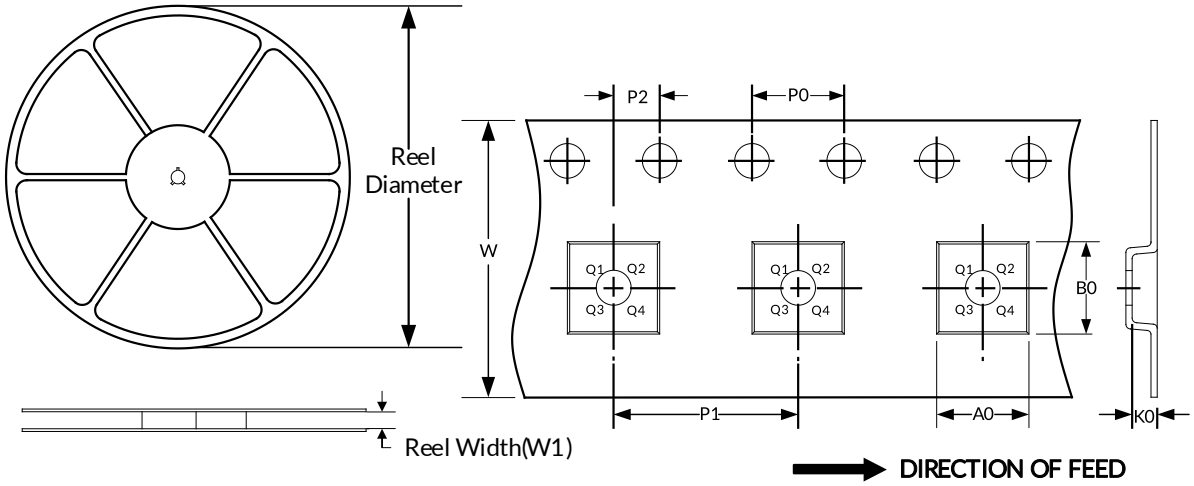
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

15 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP8	7”	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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